Fig. 32 is a plan view showing the structure of a common contact hole and another gate electrode; and

Fig. 33 is a sectional view taken along line E-E in Fig. 32.--

Kindly replace the paragraph beginning on page 9, line 12 with the following:

--The equivalent circuit diagram of Fig. 3 will next be described. Since the transistor Tr is formed in the portion where the gate electrode 30 and the device area overlap one another, the gate electrode 30, first and second diffused layers 20, 21, and well area 10 correspond to gate terminal G, source terminal S, drain terminal D, and substrate B of the transistor, respectively. The gate terminal G and source terminal S are electrically connected with the metal which covers the common contact 80. A parasitic capacitance exists between these terminals by coupling. That is, there are a capacitance Cgs drain between gate and source, a capacitance Cgd between gate and drain, a capacitance Cgb between gate and substrate, a capacitance Csb between source and substrate, and a capacitance Cdb between drain and substrate. Note that since the source terminal S and drain terminal D correspond to the impurity-diffused layers 20 and 21 which have the same structure, respectively, these terminals do not need to be especially distinguished.--

Kindly replace the paragraph beginning on page 10, line 7 with the following:

--Therefore, only the film thickness of the gate insulating film 40 in the common contact hole may be reduced as compared to that of the gate insulating film of the other

typical transistors (see Fig. 32 and 33). Moreover, the gate insulating film 40 may be formed with a material having a high dielectric constant. The relative dielectric constant of gate insulating film 40 formed with normal silicon oxide SiO_2 is about 3.8. Examples of a material having a higher relative dielectric constant than 3.8 are titanium oxide and tantalum oxide. Since the capacitance Cgb between gate and substrate is proportional to the relative dielectric constant of the insulating film 40, the additional capacitance may be increased by applying the insulating film 40 having a high dielectric constant only for the common contact 80 portion.--

Kindly replace the paragraphs on page 11, line 12 through line 21 with the following:

--In addition, there exists the advantage that using the material having a high dielectric constant only to the insulating film 40 within the common contact hole 60 not only can increase the additional capacitance, but also can suppress the increase of the delay of the transistor for switching.

In addition, there exists the advantage that increasing the impurity concentration of the first diffused layer 20 within the common contact hole 60 not only can increase the additional capacitance, but also can suppress the increase of the delay of the transistor for switching.--